## REMARKS

Claims 1-20 are pending in the application. Claims 1, 6, 11, 14, and 16 are independent. Claims 2-5 and 11-20 have been amended. It is believed that these changes introduce no new matter and their entry is respectfully requested.

### Claim Objections

In paragraph 7 of the Office Action mailed on May 6, 2004, the Examiner objected to claims 2-4, 12 and 13 because of informalities. Specifically, the Examiner requires that "fuse block voltage" in claims 2-4 be changed to "supply voltage." The Examiner further requires that "configuration signal logic" on line 1 of claim 12 be changed to "control signal" to prevent a lack of antecedent basis. The Examiner additionally requires that "configuration signal logic" on line 1 of claim 13 be changed to "control signal" and "the configuration signal logic" on line 3 of claim 13 be changed to "logic for the control signal" and "front-end logic" on line 2 of claim 13 be changed to "processor" to prevent a lack of antecedent basis. Applicants have amended claims 2-4, 12 and 13 to accommodate the objections. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the objection to claims 2-4, 12 and 13.

### Rejection of Claim 13 Under 35 U.S.C. §112, Second Paragraph

In paragraph 6 of the Office Action mailed on May 6, 2004, the Examiner rejected claims 1-5 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim that which the Applicants regards as the invention. Specifically, the Examiner states that the language "configuration signal logic" recited in line 1 and 3 of claim 13 as well as "front-end logic" recited in line 2 of claim 13 lack sufficient antecedent basis. By the foregoing Amendment, Applicants have amended claim 13 to recite "the processor of claim 11, wherein the configuration signal is coupled to inhibit booting up of the processor for a period of time after the fuse block has power." Applicants respectfully submit that this Amendment accommodates the Examiner's rejection. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the rejection to claim 13.

### Rejection of Claims 11-13 Under 35 U.S.C. §102(e) and 102(b)

In the Office Action mailed on May 6, 2004, the Examiner rejected claims 11-13 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,601,167 to Gibson et al. (hereinafter

"Gibson"). The Examiner further rejected claims 11-13 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,446,403 to Witowski et al. (hereinafter "Witowski"). Applicants respectfully traverse the Examiner's rejections. A claim is anticipated only if each and every element, as set forth in the claim, is found in a single reference. MPEP §2131; *Verdegaal Bros. v. Union Oil of California*, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). As explained below, Applicants respectfully submit that the cited references cannot anticipate these claims because each one of the cited references does not disclose every element and limitation recited in the claims.

Amended independent claim 11 now recites an apparatus comprising "a processor coupled to receive a control signal to inhibit booting up of the processor until ***a fuse block disposed in the processor and programmed with a voltage configuration signal and a frequency configuration signal to specify a processor voltage and a processor*** *clock frequency*, respectively, is determined to have a proper supply voltage level." Applicants respectfully submit that neither Gibson nor Witowski disclose, teach, or suggest a fuse block disposed in the processor and programmed with a voltage configuration signal and a frequency configuration signal to specify a processor voltage and a processor clock frequency.

Because each of the cited references fails to disclose each and every claimed element of claim 11, Applicants respectfully submit that claim 11 is not anticipated by the cited references. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the rejection of claim 11.

Regarding claims 12-13, if an independent claim is patentable, then any claim depending therefrom is also patentable. *See, e.g.,* MPEP §2143.03; *In re Fine,* 837 F.2d 1071 (Fed. Cir. 1988). Applicants therefore respectfully submit that claims 12-13 are patentable by virtue of their dependence on a patentable independent claim, as well as by virtue of the features recited in the claims. Applicants therefore respectfully request that the Examiner reconsider and remove the rejections of these claims.

Rejection of Claims 1-10 and 14-20 Under 35 U.S.C. §103(a)

In the Office Action mailed on May 6, 2004, the Examiner rejected claims 1-5 and 14-15 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,764,592 to Capps, Jr. et al. (hereinafter "Capps") in view of Witowski. The Examiner further rejected claims 6-10 and 16-20 under 35 U.S.C. §103(a) as unpatentable over Capps in view of U.S. Patent 6,275,364 to

Voit (hereinafter "Voit").

To establish a *prima facie* case of obviousness, an Examiner must show three things: (1) that there is some suggestion or motivation to modify a reference or combine reference teachings to arrive at the claimed invention, (2) that there must be a reasonable expectation of success, and (3) that the references teach or suggest each and every element of the claimed invention. (MPEP §2143). The suggestion or motivation to modify reference teachings must be found in the references relied upon (MPEP §2143.01). The proposed modification cannot render the cited reference unsatisfactory for its intended purpose, however, or change the principle of operation. (Id.) Applicants respectfully traverse the rejection.

The Examiner concedes that Capps fails to teach "a control signal coupled to the processor, the voltage regulator, and the clock generator to prevent the processor from receiving the processor voltage and the processor clock until the fuse block programmed with a voltage configuration signal and a frequency signal to specify the processor voltage and processor clock frequency, respectively, is determined to have a proper supply voltage level." More specifically, the examiner concedes that Capps is silent with respect to preventing the processor from receiving the processor voltage and processor clock.

The Examiner cites Witowski to make up for these deficiencies, arguing that it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Capps by implementing the control signal to prevent the processor from receiving the processor voltage and the processor clock as taught by Witowski. The Examiner essentially asserts that Witowski teaches a "control signal (delayed POWERGOOD signal) prevents the processor (CPU 7) from receiving the processor voltage and the processor clock until it is determined to have a proper supply voltage [Figure 7 and col. 4 line 62 et seq.]." The passage cited by the Examiner reads as follows:

> In particular, both of the control circuits utilize the POWERGOOD signal from the power supply to disable the CLOCK input to the CPU during a power-up condition. By disabling the CLOCK input of the CPU during a power-up condition, the risk of placing the internal phase-lock loop (PLL) into an illegal condition and "locking up" the system is virtually non-existent for the newer sub-micron architecture CPUs which require the CLOCK input to be held in a constant state during power-up.

(Witowski, column 4 line 62 – column 5 line 4). Applicants respectfully disagree with the Examiner's characterization of Witowski. Applicants respectfully submit that there is no disclosure, teaching, or suggestion whatsoever in this passage, nor anywhere else in Witowski,

about the use of a control signal to prevent the processor from receiving the processor voltage. Witowski cannot be fairly read to disclose, teach, or suggest inhibiting the processor voltage in response to a control signal.

Furthermore, Capps is directed to automatic frequency and voltage selection for microprocessors in a computer system. For example,

> This invention relates to a method and apparatus for providing automatic frequency and voltage selection for microprocessors in a computer system. Microprocessor identification (ID) bits are burned into a microprocessor during manufacture to specify the correct bus frequency and core voltage. A clock generator and voltage regulator receive and interpret the ID bits to provide the correct frequency and voltage.

(Capps, column 2 lines 21-28). In contrast, Witowski is directed to the use of an inhibiting clock to prevent CPUs from locking up during power-up condition. In particular,

> The present invention relates to a control circuit which inhibits the CLOCK input to the CPU during power-up conditions to prevent newer sub-micron CPUs from locking up during a power-up condition.

(Witowski, column 4 lines 8-12). Witowski apparently is not interested in frequency and voltage selection for microprocessors. Therefore such modification would ***change the intended purpose of Witowski*** and therefore is not a proper basis for an obviousness rejection.

Because the Examiner has not made out a *prima facie* case of obviousness with respect to claims 1-5 and 14-15, Applicants respectfully submit that claims 1-5 and 14-15 are patentable over the cited art. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the rejection to claims 1-5 and 14-15.

Voit appears to be directed to a method of detecting if at least one of several ports is not occupied by a device (e.g., a microprocessor) and asserting an indication to enable system operation even if the port is not occupied by a device. (Voit, column 1 lines 61-65) The problem addressed in Voit is that, where one or more of the microprocessors are removed from their sockets or connectors, the voltage regulation module ("VRM") associated with those microprocessors will drive their power good signal inactive, disabling system operation even though one or more microprocessors remain in the system. (Voit, column 1 lines 42-47). The solution proposed is to override the inactive status of the voltage valid indication provided by the VRM coupled to the unoccupied socket so that system operation is not disabled. (Voit, column 2 lines 39-42).

In the Office Action, the Examiner asserts that Voit teaches "a system that has a control signal coupled to the processor and the logic to prevent the logic from reading the configuration signal until a predetermined event occurs (VID signals reach a predetermined state) [figure 3 and col. 6 lines 6-16]. While not explicit, it would be understood that a control signal must exist to prevent the configuration signal from being read by the VRM of Voit." The passage in Voit cited by the Examiner reads as follows:

> Referring to FIG.3, a sequence of events and actions performed in the system 10 according to one embodiment is illustrated. After the system power has turned on, the CPUs 170 and 172 (if they are present) drive (at 300) their respective VID signals to predetermined states. The VID values may be programmed in non-volatile storage locations in the CPUs 170 and 172. The programmed values are driven by the CPUs 170 and 172 onto signals VID__[0:4]. And VID2__[0:4]. If one of the CPUs is not present, e.g., CPU 172, then the VID signals corresponding to the absent CPU are tied to predetermined states.

(Voit, column 6 lines 6-16) Applicants respectfully disagree with the Examiner's characterization of Voit.

Applicants respectfully submit that Voit does not teach a system that has a control signal coupled to the processor and the logic to prevent the logic from reading the configuration signal until a predetermined event occurs. As an example, Voit does not disclose a predetermined event to prevent the VRM from reading the VID signals until the occurrence of the predetermined event (i.e., the VID signals cannot prevent the VRM from reading the VID signals by themselves).

Assuming for the sake of argument, that Voit teaches what the Examiner asserts, however, the Examiner concedes that Capps fails to disclose "a control signal coupled to the processor and the logic to prevent the logic from reading the configuration signal until a predetermined event occurs." The Examiner cites Voit to make up for these deficiencies, arguing that "it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Capps by using a control signal to prevent the configuration signals from being read as taught by Voit." Applicants respectfully disagree.

Applicants respectfully submit that the combination proposed by the Examiner would ***change the principle of operation of Capps***. For example, Capps is directed toward providing automatic frequency and voltage selection for microprocessors in a computer system, which requires the actual presence of the microprocessor. In contrast, Voit is directed toward enabling

system operation in system when one or more microprocessors are missing from the system. This is contrary to the operating principles of Capps and is thus not a proper basis for an obviousness rejection.

Because the Examiner has not made out a *prima facie* case of obviousness with respect to claims 6-10 and 16-20, Applicants respectfully submit that claims 6-10 and 16-20 are patentable over the cited art. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the rejection to claims 6-10 and 16-20.

## CONCLUSION

Applicants submit that all grounds for objection and rejection have been properly traversed, accommodated, or rendered moot and that the application is now in condition for allowance. The Examiner is invited to telephone the undersigned representative if the Examiner believes that an interview might be useful for any reason.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: August 6, 2004

Jan Little-Washington
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